REMARKS

This application has been reviewed in light of the Office Action dated December 12, 2001. Claims 13-16 remain pending in this application. Claims 13 and 15, the independent claims, have been amended to recite Applicant's invention more clearly. Favorable reconsideration is requested.

The Office Action rejected Claims 13-16 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,745,485 (Iwasaki) in view of U.S. Patent No. 4,864,402 (Ebihara et al.)

Applicant submits that independent Claims 13 and 15 along with their respective dependant claims, are patentably distinct from the cited prior art for at least the following reasons.

Claim 13 recites, inter alia, a memory controller comprising a serial/parallel converter section for converting bit width 'a' of an input data signal, into a width a*N long where N is ≥4, a first FIFO memory a*N bits wide for temporarily storing the signal after it has been subjected to serial/parallel conversion, a SDRAM with the capacity of a single frame for reading data at the same frequency of the input data after storing a predetermined quantity, a*N*L (where L is an integer), of data into the first FIFO memory, and for storing data read out of the first FIFO memory, a memory controller for reading from and writing into the SDRAM by driving successively as a single block, a second FIFO memory having a width a*N for reading from the SDRAM at the same frequency as the input data and for temporarily storing the data in such a way that after storing the data of a predetermined quantity 2*a*N*L into the second FIFO

memory, the data is read at a frequency half of the frequency of the input data. A continuous period of writing into and reading from the SDRAM is designed as an L cycle, a single time of continuous writing period and two times of continuous reading period are performed during a period N*L, an instruction period (including latency) instructing the memory necessary for performing continuous access to the SDRAM is the same as or shorter then a remaining period, N*L-3*L, so that the first FIFO size is set as a*N*L bits, and the second FIFO size is set as a*N*2*L bits.

Iwasaki, as understood by the Applicant, contains a serial/parallel converter (column 3, lines 20-22) with a fixed width of 8 bits. However, Applicant has found no teaching or suggestion of, inter alia, the serial/parallel converter of Claim 13, which is used for converting bit width 'a' (where 'a' is a positive number) of an input data signal into a width N times ($N \geq 4$) as long as 'a'.

Applicant understands Ebihara et al. to contain a cyclic-type filter used for noise reduction (column 5, lines 49-52). Ebihara et al. is also not believed to remedy the above mentioned deficiency of Iwasaki as a reference against Claim 13. Accordingly, Claim 13 is believed patentable over the cited references.

As shown above, Claims 13 and 15 have been amended to define still more clearly Applicant's invention. Neither Iwasaki nor Ebihara is believed to teach or suggest the use of an SDRAM as a frame memory. For at least this additional reason, independent Claims 13 and 15 are patentably distinct over the cited art.

Moreover, Applicant disagrees with the position taken in the Office Action that Ebihara et al. provided the continuous period of writing into and reading from the frame memory as recited in Claim 13. The invention recited in Claim 13 creates a continuous, and not cyclical, read write period, due to the fact that the writing speed of the FIFO, into the frame memory (now more clearly defined as an SDRAM) is higher then the reading speed out of the FIFO. As a result of this difference, reading the data out of SDRAM frame memory can be conducted within the time period used to write such memory or within double the time period. In contrast, Ebihara et al. teaches a cyclic-type filter (col. 5, lines 49-51), used to achieve a noise reduction function.

Applicant submits that Ebihara's cyclic period feature is used to reduce noise and does not teach or suggest providing a frame memory, including an SDRAM, with a continuous period of writing into and reading from the frame memory, as is recited.

Independent Claim 15 recites an SDRAM frame memory, a substantially similar serial/parallel converting section as well as the continuous read write feature recited in Claim 13. Therefore independent Claim15 is submitted to be patentable for at least the same reasons as discussed above in connection with Claim 13.

The other claims rejected depend from one or another of the independent claims discussed above and, therefore, are submitted to be patentable for at least the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, individual reconsideration of the patentability of each claim on its own merits is respectfully requested.

In view of the foregoing remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE TO CLAIMS

13. (Amended) A memory controller comprising:

a serial/parallel converter section for converting bit width a (where a is a positive number) of an input data signal into a width N times ($N \geq 4$) as long as a;

a first FIFO memory of a*N bits in width for storing temporarily the signal after it has been subjected to the serial/parallel conversion; and

a [frame memory] SDRAM having a capacity of a single frame for reading data at the same frequency as the input frequency of the input data after storing a predetermined quantity, a*N*L bits (where L is an integer), of the data into said first FIFO memory, and for storing the data read out from said first FIFO memory;

a memory controller for reading from and writing into said [frame memory] SDRAM by driving successively as a single block;

a second FIFO memory having width a*N for reading from said [frame memory] SDRAM at the same frequency as the input data and for storing temporarily the data, such that, after storing data of a predetermined quantity 2*a*N*L into said second FIFO memory, the data is read at a frequency a half of the frequency of the input data, wherein

a continuous period of writing into and reading from said [frame memory] SDRAM is designed as an L cycle, a single time of continuous writing period and two times of continuous reading period are performed during a period N*L, an instruction period (including latency) instructing the memory necessary for performing continuous access to the [frame memory] SDRAM is the same as or shorter than a remaining period, N*L-3*L, so that a first FIFO size is set as a*N*L bits, and a second FIFO size is set as a*N*2*L bits.

15. (Amended) A memory controller comprising:

a serial/parallel converter section for converting bit width a (where a is a positive number) of an input data signal into an width M times ($M \geq 4$) as long as a;

a first FIFO memory of a*M bit width for storing temporarily the signal after it has been subjected to the serial/parallel conversion; and

a [frame memory] SDRAM having a capacity of a single frame for reading data at a frequency half of the input frequency of the input data after storing a predetermined quantity, a*M*L bits (where L is integer), of the data into said first FIFO memory, and for storing the data read out from said first FIFO memory;

a memory controller for reading from and writing into said [frame memory] SDRAM by driving successively as a single block;

a second FIFO memory having width a*M for reading from said [frame memory] SDRAM at a frequency half of the frequency of the input data and for storing temporary the data, such that, after storing data of a predetermined quantity 2*a*M*L into said second FIPO memory, the data is read at a frequency a half of the frequency of the input data, wherein

a continuous period of writing into and reading from said [frame memory] SDRAM is designed as an L cycle, a single time of continuous writing period and two times of continuous reading period are performed during a period M*L, an instruction period (including latency[,]) instructing the memory necessary for performing continuous access to the [frame memory] SDRAM is the same as or shorter than a remaining period, M*L-3*L, so that a speed of accessing said [frame memory] SDRAM is less than 1/2 of the data input speed.